| Notice of Allowability | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/058,651 | BLUMENAU ET AL. | |
| | Examiner | Art Unit | |
| | Kyung H. Shin | 2143 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--*

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *9/16/05 & phone interviewed on 4/11/06*.

2. ☒ The allowed claim(s) is/are *1-12*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   **Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *4/11/06* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

WILLIAM C. VAUGHN, JR.
PRIMARY EXAMINER

## DETAILED ACTION

### *Response to Amendment*

1. **Claims 1 - 12** are pending. Independent Claims are **1, 7, 12**.

## EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with RICHARD AUCHTERLONIE: Reg. No. 30,607, (713) 751-0655 on 4/11/2006.

3. The application has been amended as follows:

In Claims:

1. An electronic circuit chip comprising:

a memory for storing information defining an encryption procedure assigned to the electronic circuit chip;

at least one input to the electronic circuit chip for writing, to the memory, the information defining the encryption procedure assigned to the electronic circuit chip, and for receiving data to be encrypted by the encryption procedure assigned to the electronic circuit chip;

encryption circuitry for reading from the memory the information defining the encryption procedure assigned to the electronic circuit chip, and for encrypting the data from said at least one input to the electronic circuit chip according to the encryption procedure assigned to the electronic circuit chip, to produce encrypted data; and

at least one output from the electronic circuit chip for transmitting the encrypted data produced by the encryption circuitry;

wherein the electronic circuit chip is constructed so that the information defining the encryption procedure assigned to the electronic circuit chip cannot be read from the memory from any output of the electronic circuit chip; and

wherein the electronic circuit chip is constructed so that it cannot recover the information in the memory by probing, inspection, or disassembly; and

which includes a metal shielding layer over the memory so that the information stored in the memory cannot be read by visual inspection or probing.

7. An electronic circuit chip comprising:

a memory for storing information;

a microprocessor coupled to the memory for reading information from the memory;

at least one input to the electronic circuit chip for receiving information to be written to the memory, and for receiving data to be processed by the microprocessor; and

at least one output from the electronic circuit chip for transmitting data processed by the microprocessor;

wherein the electronic circuit chip is constructed so that information can be stored in the memory but not read from any output of the electronic circuit chip, and the microprocessor is programmable for encrypting data in accordance with an encryption procedure defined by information that can be stored in the memory but not read from any output of the electronic circuit chip;

wherein the electronic circuit chip is constructed so that it cannot recover the information in the memory by probing, inspection, or disassembly; and

which includes a metal shielding layer over the memory so that the information stored in the memory cannot be read by visual inspection or probing.

12. An electronic circuit chip comprising:

a memory for storing information;

a microprocessor coupled to the memory for reading information from the memory;

at least one input to the electronic circuit chip for receiving information to be written to the memory, and for receiving data to be processed by the microprocessor; and

at least one output from the electronic circuit chip for transmitting data processed by the microprocessor;

wherein the electronic circuit chip is constructed so that information can be stored in the memory but not read from any output of the electronic circuit chip, and the microprocessor is programmable for encrypting data in accordance with an encryption procedure defined by information that can be stored in the memory but not read from any output of the electronic circuit chip;

wherein the electronic circuit chip is constructed so that it cannot recover the information in the memory by probing, inspection, or disassembly; and

which includes a metal shielding layer over the memory so that the information stored in the memory cannot be read by visual inspection or probing;

wherein the electronic circuit chip is a monolithic semiconductor integrated circuit chip, the memory is an electrically erasable and programmable read-only memory, and the metal shielding layer over the memory is an upper layer of metal on the electronic circuit chip; and

wherein the microprocessor is programmed to read an encryption key from the memory, and to compute the encrypted data using the encryption key, and the encryption key defines the encryption procedure assigned to the electronic circuit chip.

***Allowable Subject Matter***

4. The following is an Examiner's statement of reasons for allowance.

- The Jones (6,088,800) prior art discloses "a programmable electronic circuit chip utilized for data encryption".

- The Best (4,465,901) prior art discloses "an electronic circuit chip with the capability, whereby it is impossible to recover information from the chip by probing, inspection, or disassembly".
- The Rigal (5,881,155) prior art discloses "a metal shielding covering the electronic circuit chip". and
- Little (5,998,858) discloses "an electronic circuit chip with an electronically erasable and programmable read only memory".

Applicant discloses in Independent claims 1, 7, 12, an encryption chip with a metal shielding layer over the memory. (see Remarks dated September 16, 2005 Page 11, Lines 10-12) The closest prior art of record, the Jones (6,088,800) and Rigal (5,881,155) prior art combination discloses a metal shielding layer specifically covering the encryption chip and formed at the periphery of the chip, whereby portions of the ring do not overlap the entire chip.

After extensive searching and analysis of prior art in light of the Applicant's claimed invention, the Examiner finds that the referenced prior art does not teach or suggest in detail the invention's disclosure in combination with all the elements of each independent claim as argued by the Applicant. So as indicated by the above statements, Applicant's arguments have been considered persuasive, in light of the claim limitations as well as the enabling portions of the specification.

5. The dependent claims further limit the independent claims and are considered allowable on the same basis as the independent claims as well as for the further

limitations set forth. Any comments considered necessary by Applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kyung H. Shin whose telephone number is (571) 272-3920. The examiner can normally be reached on 7:30 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David A. Wiley can be reached on (571) 272-3923. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KHS
Kyung H Shin 4-11-06
Patent Examiner
Art Unit 2143

WILLIAM C. VAUGHN, JR.
PRIMARY EXAMINER